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15EC655

Sixth Semester B.E. Degree Examination, Aug./Sept.2020
Microelectronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Derive the expression of drain current of an NMOS transistor when it operates in triode and saturation regions. **(10 Marks)**

b. The PMOS transistor shown in Fig.Q1(b) has $V_t = -1V$, $K'_p = 60\ \mu A/V^2$ and $\frac{W}{L} = 10$. Find the range of V_G for which the transistor conducts and also, in terms of V_G, find the range of V_D for which the transistor operates in triode region.

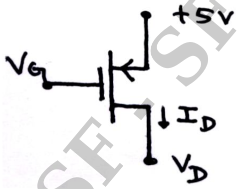

Fig.Q1(b) **(03 Marks)**

c. An NMOS transistor has $V_{to} = 0.8$ V, $2\phi_f = 0.7V$ and $\gamma = 0.4\ V^{1/2}$. Find V_t when $V_{SB} = 3V$. **(03 Marks)**

OR

2 a. An NMOS transistor is fabricated in a 0.4 μm process having $\mu_n C_{ox} = 200\ \mu A/V^2$ and $V'_A = 50$ V/μm. If L = 0.8 μm and W = 16 μm, find V_A and λ. Find the value of I_D that results when the device is operated with an overdrive voltage, $V_{OV} = 0.5$ V and $V_{DS} = 1V$. **(04 Marks)**

b. Analyze the circuit shown in Fig.Q2(b) and hence determine the voltages at all nodes and the currents through all branches. Neglect channel length modulation effect. Let, $V_t = 1V$ and $K'_n W/L = 1mA/V^2$.

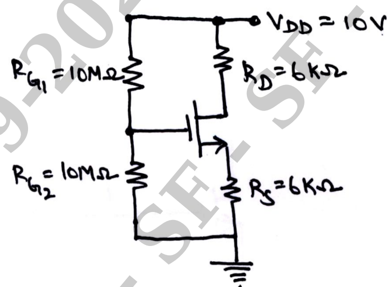

Fig.Q2(b) **(06 Marks)**

c. Sketch the transfer characteristic of the common source amplifier shown in Fig.Q2(c). Identify the segments related to three regions of operation of the device. Also, obtain the expression of incremental voltage gain, A_V.

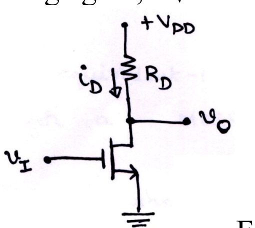

Fig.Q2(c) **(06 Marks)**

Module-2

3 a. Discuss the MOSFET biasing that uses a drain-to-gate feedback resistor. **(04 Marks)**

b. For the discrete common-source MOSFET amplifier shown in Fig.Q3(b), write the equivalent circuit used to determine the low frequency response. Also, obtain the expressions of pole-frequencies of the response.

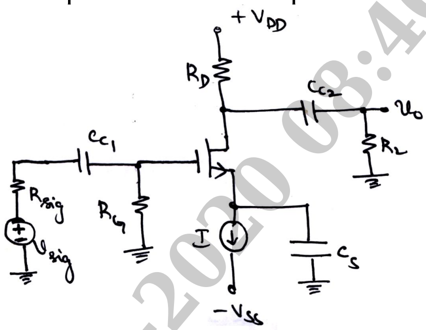

Fig.Q3(b) **(08 Marks)**

c. A drain current of 0.5 mA is observed when a gate-source voltage of 2V is applied to NMOS. Drain current increases to 0.55 mA when gate source voltage of 2.05V is applied. Find the value of device transconductance, g_m. Also obtain, threshold voltage, V_t, if $K_n' W/L = 1\ mA/V^2$. **(04 Marks)**

OR

4 a. Obtain T equivalent circuit model from hybrid-π model for a MOSFET. **(04 Marks)**

b. For the circuit shown in Fig.Q4(b), find the value of V_{GS} such that $I_D = 0.5$ mA. The device parameters are $V_t = 1V$ and $K_n' W/L = 1\ mA/V^2$. What is the percentage change in ID obtained when the transistor is replaced by another having $V_t = 1.5$ V? Comment on the change in I_D.

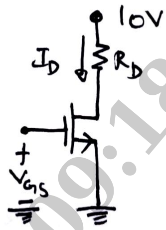

Fig.Q4(b) **(04 Marks)**

c. Derive the expression of the MOSFET Unity-gain frequency, f_T. **(08 Marks)**

Module-3

5 a. Draw the circuit of discrete common-source amplifier with a source resistance. Derive the expressions for R_{in}, A_v and G_v. **(10 Marks)**

b. Derive an approximate formula for 3-dB frequency, ωH, of a direct-coupled amplifier, when a dominant pole does not exist in the gain function of amplifier. **(06 Marks)**

OR

6 a. Draw and explain the operation of MOS current-steering circuits. **(08 Marks)**

b. Consider a source follower shown in Fig.Q6(b). Note that gm = 1 mA/V, r_0 = 150 KΩ, R_{sig} = 1 MΩ, RG = 4.7 MΩ and RL = 15 KΩ. Find R_{in}, Av, Rout and G_v of the circuit.

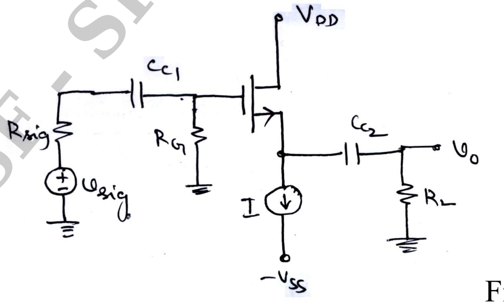

Fig.Q6(b) **(08 Marks)**

Module-4

7 a. Derive the expressions of input and output resistances of common-gate amplifier with active load. **(10 Marks)**

b. Draw the high frequency equivalent circuit of common source amplifier with current source as load. Analyze the same to determine 3-dB frequency, f_H, using the open-circuit time constant method. **(06 Marks)**

OR

8 a. Consider CMOS implementation of common-source amplifier. Let, $V_{DD} = 3V$, $V_{tn} = |V_{tp}| = 0.6V$, $\mu_n C_{ox} = 200\ \mu A/V^2$ and $\mu_p C_{ox} = 65\ \mu A/V^2$. Also, for all transistors, L = 0.4 μm and W = 4μm. If $V_{An} = 20$ V, $|V_{Ap}| = 10$ V and $I_{REF} = 10\ \mu A$, find the small-signal voltage gain. **(06 Marks)**

b. Obtain the expressions of output resistance, Rout, open-circuit voltage gain, A_{vo} and short-circuit transconductance, G_m, of MOS cascade amplifier. **(10 Marks)**

Module-5

9 a. Explain the operation of passive-loaded MOS differential pair for a differential input voltage. **(08 Marks)**

b. Sketch the equivalent circuit of active-loaded MOS differential pair used for frequency response analysis. Derive the expression of transfer function. **(08 Marks)**

OR

10 a. Obtain the expression of common-mode rejection ratio (CMRR) of passive-loaded MOS differential pair, by considering the effect of R_D mismatch. **(07 Marks)**

b. Explain the operation of two-stage CMOS OP-AMP. Write the expressions of DC voltage gains, of the individual stages and the overall configuration. **(09 Marks)**

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